

PRELIMINARY AMENDMENT

Serial Number: Unknown

Filing Date: Unknown

Title: SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT

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Dkt: 703.019US3

B7
Encl

77. (New) The method of claim 75, wherein a first well isolating the first transistor from a substrate of the integrated circuit is coupled to the first source/drain and gate of the second transistor and wherein a second well isolating the second transistor from a substrate of the integrated circuit is coupled to the at least one internal circuit.

REMARKS

Claims 1, 6 and 15 are canceled and claims 22-77 have been added. Accordingly, claims 22-77 are currently pending in the application.

Respectfully submitted,

CHRISTOPHER J. CHEVALLIER

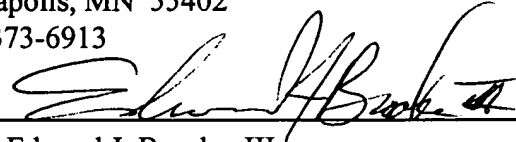
By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date

11/1/2001

By



Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 21st day of November 2001.

Name

Amy Moriarty

Signature

Amy Moriarty